WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

forming a resist post on a connection pad of a semiconductor chip;

forming an insulating layer that covers the semiconductor chip and the resist post;

removing a part of the insulating layer to expose a surface of the resist post;

removing the resist post to form a through hole in the insulating layer, the through hole thereby exposing the connection pad; and

forming a wiring layer that is in electrical contact with the connection pad via the through hole and is elongated over the insulating layer.

2. A method according to claim 1, wherein the wiring layer is formed by plating.

3. A method according to claim 1, further comprising:

connecting a circuit board and the insulating layer having the wiring layer after forming the wiring.

4. A method according to claim 1, further comprising:

connecting a support member to a rear surface of the semiconductor chip that is on the side opposite to a surface on which the connection pad is formed, after forming the resist post; and

removing the support member after forming the wiring layer.

5. A method according to claim 1, wherein the resist post has a shape whose horizontal cross sectional area becomes larger from a bottom surface of the resist post contacting the connection pad toward the other surface of the resist post that is on the side opposite to the bottom surface.

6. A method according to claim 1, wherein a value found by dividing the depth of the through hole by a reduced radius for a surface that is parallel to an opening surface of the through hole and that has a maximum surface area is equal to or greater than 1.

7. A method according to claim 1, further comprising:

forming a groove in a front surface of the insulating layer, after exposing the surface of the resist post, wherein the groove is connecting to the through hole, and a part of the wiring layer is embedded in the groove.

8. A method for manufacturing a semiconductor device, comprising:

forming a first resist post on a connection pad of a semiconductor chip;

forming a second resist post on a support member;

mounting the semiconductor chip on the support member apart from the second resist post;

forming an insulating layer that covers the semiconductor chip, the first resist post, and the second resist post;

removing the insulating layer to expose a surface of the first resist post and a surface of the second resist post;

removing the first resist post and the second resist post to form a first through hole and a second through hole in the insulating layer, the first through hole thereby exposing the connection pad, and the second through hole thereby exposing the support member;

forming a wiring layer that is in electrical contact with the connection pad via the first through hole and is in contact with the support member via the second through hole and is elongated over the insulating layer; and

removing at least a part of the support member to expose the wiring layer as a rear pad in a surface of the insulating layer opposite to a surface in which the first through hole is formed.

9. A method according to claim 8, wherein the wiring layer is formed by plating.

10. A method according to claim 8, further comprising:

preparing a plurality of the semiconductor devices;

connecting the rear pad of one of the semiconductor devices to the wiring layer of another

semiconductor device electrically to laminate the plurality of the semiconductor devices .

11. A method according to claim 10, wherein the rear pad of one of the semiconductor devices and the wiring layer of another semiconductor device are connected via a solder bump or a conductive paste.

12. A method according to claim 8, further comprising:

preparing a plurality of the semiconductor devices;

forming a build-up multi-layer substrate on the wiring layer of each of the semiconductor devices, the build-up multi-layer substrate having a connection portion on a surface opposite to a surface facing the wiring layer;

connecting the rear pad of one of the semiconductor devices to the connection portion of the build-up multi-layer substrate formed on another semiconductor device electrically to laminate the plurality of the semiconductor devices.

13. A semiconductor apparatus having a first semiconductor device,

said first semiconductor device comprising:

a first semiconductor chip having a first front surface having thereon a first connection pad and a first back surface opposing to said first front surface;

a first resin body encapsulating said first semiconductor chip with leaving said first back surface of said semiconductor chip exposed from said first resin body,

said first back surface of said first semiconductor chip being thereby in substantially same plane as a surface of said first resin body;

a first through hole selectively formed in said first resin body to expose a part of said first connection pad;

a second through hole penetrating said first resin body; and

a first conductive layer connected to said part of said first connection pad via said first through hole, elongated over said first resin body, inserted in said second through hole and terminated to be in substantially same plane as the surface of said first resin body.

14. The apparatus as claimed in claim 13, wherein each of said first and second through holes is filled up with said first conductive layer.

15. The apparatus as claimed in claim 14, wherein said first conductive layer is formed continuously over a whole area by said first conductive layer being formed in one time.

16. The apparatus as claimed in claim 13, further comprising a second semiconductor device and a conductor,

said second semiconductor device comprising:

a second semiconductor chip having a second front surface having thereon a second connection pad and a second back surface opposing to said second front surface;

a second resin body encapsulating said second semiconductor chip with leaving said second back surface of

said second semiconductor chip exposed from said second resin body, said second back surface of said second semiconductor chip being thereby in substantially same plane as a surface of said second resin body;

a third through hole selectively formed in said second resin body to expose a part of said second connection pad;

a fourth through hole penetrating said second resin body; and

a second conductive layer connected to said part of said second connection pad via said third through hole, elongated over said second resin body, inserted in said fourth through hole and terminated to be in substantially same plane as the surface of said second resin body;

said first semiconductor device being stacked on said second semiconductor device with an intervention of said conductor which electrically connects said first conductive layer to said second conductive layer.

17. The device as claimed in claim 16, wherein each of said first and second through holes is filled up with said first conductive layer and each of said third and fourth through holes is filled up with said second conductive layer.

18. The apparatus as claimed in claim 17, wherein said first conductive layer is formed continuously over a whole area by said first conductive layer being formed in one time and said second conductive layer is formed

continuously over a whole area by said second conductive layer being formed in one time.